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EXAMINER	
PARK, ILWOO	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 10

Application Number: 09/432,819
Filing Date: November 02, 1999
Appellant(s): RHEE, QUE-WON

Douglas L. Weller
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/9/2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1, 2, 4, and 6-12 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,870,310 MALLADI 2-1999

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 2, 4, and 6-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Malladi, US patent No. 5,870,310.

As to claim 1, Malladi teaches an interface block [e.g., data processing shells 141a-141c, 141b', 301, 327, or 337 in figs. 1-3] that provides an interface [col. 2, lines 3-9] between an internal bus [CPU bus] and a socket [memory bus] of a logic block [e.g., memory shell 122 or 122', memory controller 322, or display controller unit 352 in figs. 1-3], the interface block, the internal bus and the logic block all being located within a single integrated circuit [system-on-a-chip: col. 1, line 57-col. 2, line 3], the interface block comprising:

a synchronization module [interface logic cell for timing requirements: col. 2, lines 3-9, e.g., memory interface units 150a-150c, 250b, 312, 326, or 336 in figs. 1-3] that performs any needed synchronization [timing requirements in col. 2, lines 3-9] between a clock domain [e.g., various clock of Pentium, PowerPC, SPARC, or MIPS processor in col. 3, lines 42-48] of the internal bus and a clock domain [e.g., various clock of ISA, AT ISA, PCI, EISA, or MCA bus in col. 4, lines 43-56] of the socket of the logic block;

a translation module [additional interface logic cell for communication protocols: col. 5, lines 2-7] that, for data transferred between the internal bus and the socket of the logic block, provides translation of block encoding of the data;

a queue module [additional interface logic cell for buffers: col. 5, lines 2-7] that buffers [col. 8, lines 61-66] data flowing between the internal bus and the socket of the logic block; and

a driver module [e.g., bus interface units 140a-140c, 240b, 310, 336, or 340 in figs. 1-3] that handles [col. 4, lines 62-65 and col. 4, lines 35-38] low level and electrical drive specifications of the internal bus.

As to claim 2, Malladi teaches the synchronization module can be implemented as one of:

a null synchronization block where no synchronization is required between the clock domain of the internal bus and the clock domain of the socket of the logic block;

a ratio synchronization block where the clock domain of the internal bus is related to the clock domain of the socket of the logic block by a fixed multiplier ratio; and

a full synchronization block where there is no phase relationship between the clock domain [col. 3, lines 42-48; e.g., 100 MHz PowerPC 603] of the internal bus and the clock domain [col. 4, lines 43-56: e.g., 8 MHz AT/ISA] of the socket of the logic block.

As to claim 4, Malladi teaches a method for providing an interface [col. 2, lines 3-9] between an internal bus [CPU bus] of an integrated circuit [system-on-a-chip: col. 1, line 57-col. 2, line 3] and a socket [memory bus] of a logic block [e.g., memory shell 122 or 122', memory controller 322, or display controller unit 352 in figs. 1-3] within the integrated circuit, the method comprising the steps of:

a) performing any needed synchronization [timing requirements in col. 2, lines 3-9] between a clock domain [e.g., various clock of Pentium, PowerPC, SPARC, or MIPS processor in col. 3, lines 42-48] of the internal bus and a clock domain [e.g., various clock of ISA, AT ISA, PCI, EISA, or MCA bus in col. 4, lines 43-56] of the socket of the logic block within a synchronization module [interface logic cell for timing requirements: col. 2, lines 3-9, e.g., memory interface units 150a-150c, 250b, 312, 326, or 336 in figs. 1-3];

b) performing any required translation of block encoding of data transferred between the internal bus and the socket of the logic block using a translation module [additional interface logic cell for communication protocols: col. 5, lines 2-7];

c) buffering data [col. 8, lines 61-66] flowing between the internal bus and the socket of the logic block using a queue module [additional interface logic cell for buffers: col. 5, lines 2-7]; and

d) handling [col. 4, lines 62-65 and col. 4, lines 35-38] low level and electrical drive specifications of the internal bus using a driver module [e.g., bus interface units 140a-140c, 240b, 310, 336, or 340 in figs. 1-3].

As to claim 6, Malladi teaches providing buffers between modules to allow pipelined operation [col. 8, lines 61-66].

As to claim 7, Malladi teaches on an integrated circuit [system-on-a-chip: col. 1, line 57-col. 2, line 3], an interface block [e.g., data processing shells 141a-141c, 141b', 301, 327, or 337 in figs. 1-3] that provides an interface [col. 2, lines 3-9] between an internal bus [CPU bus] of the integrated circuit and a socket [memory bus] of a logic

block [e.g., memory shell 122, memory controller 322, or display controller unit 352 in figs. 1-3], the interface block comprising:

a plurality of modules [e.g., logic cells 140a, 108, 150a inside of shell 141a, logic cells 140b, 110, 150b inside of shell 141b, logic cells 240b, 110, 250b inside of shell 141b', logic cells 302, 304, 308 inside of shell 301, logic cells 302, 306, 312 inside of shell 301, logic cells 310, 306, 312 inside of shell 301, logic cells 336, 328, 332, 334, 326 inside of shell 327, logic cells 340, 342, 344, 346 inside of shell 337, or logic cells 340, 338, 336 inside of shell 337] connected in series [see figs. 1-3], wherein each module in the plurality of modules performs only a single function [col. 4, lines 52-56; col. 5, lines 2-7; col. 6, line 34-col. 7, line 19] from a plurality of functions;

wherein any needed synchronization [by an interface logic cell for timing requirements: col. 2, lines 3-9, e.g., memory interface units 150a-150c, 250b, 312, 326, or 336 in figs. 1-3] between a clock domain [e.g., various clock of Pentium, PowerPC, SPARC, or MIPS processor in col. 3, lines 42-48] of the internal bus and a clock domain [e.g., various clock of ISA, AT ISA, PCI, EISA, or MCA bus in col. 4, lines 43-56] of the socket of the logic block is a first function from the plurality of functions, any required translation [by an additional interface logic cell for communication protocols: col. 5, lines 2-7] of block encoding of data is a second function from the plurality of functions, any buffering of data [by an additional interface logic cell for buffers: col. 5, lines 2-7 and col. 8, lines 61-66] flowing between the internal bus and the socket of the logic block is a third function from the plurality of functions, and handling [e.g., bus interface units 140a-140c, 240b, 310, 336, or 340 in figs. 1-3, col. 4, lines 62-65, and col. 4, lines 35-38] any

low level and electrical drive specifications of the internal bus is a fourth function from the plurality of functions.

As to claim 8, Malladi teaches a first module in the plurality of modules is a synchronization module [interface logic cell for timing requirements: col. 2, lines 3-9, e.g., memory interface units 150a-150c, 250b, 312, 326, or 336 in figs. 1-3] that performs any needed synchronization between the clock domain of the internal bus and the clock domain of the socket of the logic block within a synchronization module.

As to claim 9, Malladi teaches one module in the plurality of modules is a translation module [additional interface logic cell for communication protocols: col. 5, lines 2-7] that, for data transferred between the internal bus and the socket of the logic block, provides translation of block encoding of the data.

As to claim 10, Malladi teaches one module in the plurality of modules is a queue module [additional interface logic cell for buffers: col. 5, lines 2-7 and col. 8, lines 61-66] that buffers data flowing between the internal bus and the socket of the logic block.

As to claim 11, Malladi teaches one module in the plurality of modules is a driver module [e.g., bus interface units 140a-140c, 240b, 310, 336, or 340 in figs. 1-3 and col. 4, line 62-col. 5, line 2] that handles low level and electrical drive specifications of the internal bus.

As to claim 12, Malladi teaches providing a plurality of buffers situated between modules in the plurality of modules, the buffers used to pipeline [col. 8, lines 61-66] the interface block.

(11) Response to Argument

The Examiner summarizes the various points raised by the Appellants and addresses replies individually.

A) In section C.1 of pages 5-6 of the Appeal Brief, the Appellants argument in substance that **a)** even though Malladi does disclose interface logic cells [e.g., 116a] that can be used as an interface between an internal bus [CPU bus 100] and a logic block [CPU core A 104] while the Appellant repeatedly, in sections C.1, C.2, E.1, E.2, F.1, and F.2, tries to treat logic cells [e.g., 116a, 140a, 140b, 140c, 150a, 150b, 150c, 250b, 312, 326, or 336] of Malladi corresponds to an interface between a logic core and a bus of the claim and seeks the claim limitations including modules, functions, or connections out of the logic cells, and **b)** Malladi does not give any indication that the disclosed interface logic cells are modular:

for point a), as the Examiner clearly, in here (*vide supra*) and the last office action (mailed on 2/4/2003), states that the interface block [e.g., data processing shells 141a-141c, 141b', 301, 327, or 337] between an internal bus [CPU bus] and a socket[1] [memory bus] of a logic block [e.g., memory shell 122 or 122', memory controller 322, or display controller unit 352] while the Appellant repeatedly fails to provide explanations of

[1] The socket is a bus comprising control lines and data lines as defined and supported in page 1, lines 5-7 of the specification and page 3 of the appeal brief.

the each of logic cells interfacing between a socket of logic block and an internal bus; and **for point b)**, Malladi teaches that the interface logic shells are modular[2].

B) In section C.2 of pages 7-8 of the Appeal Brief, the Appellants argument in substance that **c)** the Examiner made incorrect correlations between the claim and entities within Malladi includes, for example, a synchronization module (e.g., MIUs 150a-150c) and a driver module (e.g., BIUs 140a-140c) are not within the same interface block and do not even interface to the same bus and **d)** the Examiner asserting memory interface units 150a-150c are examples of translation modules in the Office Action dated February 4, 2003 at page 3, lines 7-8:

for point c), Malladi teaches, for example, a synchronization module [e.g, MIU 150a] and a driver [BIU 140a] are within the same interface block [shell 141a] and interface to the same bus [CPU bus 100], a synchronization module [e.g, MIU 150b] and a driver [BIU 140b] are within the same interface block [shell 141b] and interface to the same bus [CPU bus 100], or a synchronization module [e.g, MIU 336] and a driver [BIU 340] are within the same interface block [shell 337] and interface to the same bus [CPU bus 316], etc.; and **for point d)**, the Examiner asserts additional cells for communication protocols are examples of translation modules in here (*vide supra*) and in the last office action (mailed on 2/4/2003).

[2] Each of shells/cores/cells is a module because each of them is stored in the library as a unit or module [col. 1, lines 41-65], can be selected or re-useable [col. 5, lines 28-35] as needed [col. 5, lines 2-9].

C) In sections D.1, D.2, and E.1 of pages 9-12 of the Appeal Brief, the Appellants argument in substance that **e)** Malladi does not disclose a synchronization module and does not disclose a synchronization module being implemented as a null synchronization block, a ratio synchronization block, or a full synchronization block and **f)** does not provide a further explanation of a null synchronization block or a ratio synchronization block:

for point e), Malladi teaches a synchronization module being implemented as full synchronization block for timing requirements as needed between the CPU [e.g., Pentium, PowerPC, SPARC, or MIPS processor] bus and the memory bus [ISA, AT ISA, PCI, EISA, or MCA bus]; and **for point f)**, the claim 2 requires one of a null synchronization block, a ratio synchronization block, or a full synchronization block[3] and Malladi teaches a synchronization module being implemented as full synchronization block.

D) In sections F.1 and F.2 of pages 13-14 of the Appeal Brief, the Appellants argument in substance that **g)** nowhere in Malladi disclosed an interface block that comprises a plurality of modules connected in series:

for point g), Malladi teaches an interface block that comprises a plurality of modules [e.g., logic cells 140a, 108, 150a inside of shell 141a, logic cells 140b, 110, 150b inside of shell 141b, logic cells 240b, 110, 250b inside of shell 141b', logic cells 302, 304, 308 inside of shell 301, logic cells 302, 306, 312 inside of shell 301, logic cells

[3] For example, there is no phase relationship between the CPU bus, such as PowerPC 603 operating at 100 MHz and the memory bus, such as AT ISA operating at 8 MHz.

310, 306, 312 inside of shell 301, logic cells 336, 328, 332, 334, 326 inside of shell 327, logic cells 340, 342, 344, 346 inside of shell 337, or logic cells 340, 338, 336 inside of shell 337] connected in series.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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August 6, 2003

Conferees

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